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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,091	11/28/2001	Hayden Clavie Cranford JR.	RAL920010004US2 (IRA-10-5	2524

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/996,091	CRANFORD ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 29 November 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See attached Response to Arguments*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: _____.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 29 November 2004 have been fully considered but they are not persuasive.

2. Applicant has argued that Shohara does not "teach or suggest the use of a phase rotator for edge detection". The Examiner notes that Claims 1 and 11 do not require the phase rotator to perform edge detection. Claim 1 recites "using a phase rotator to convert said asynchronous signal to said synchronous digital parallel data *in conjunction with* said edge detection" (emphasis added). Similarly, Claim 11 recites "said circuitry to restore said asynchronous signal to said synchronous digital data including a phase rotator *to act in conjunction with* the circuitry to detect both edges" (emphasis added). It is noted that the features upon which Applicant relies (i.e., the phase rotator performing edge detection) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Shohara teaches a phase rotator (See Figure 1 Number 20) that is used in conjunction with an analog to digital converter (See Figure 1 Number 18) in order to convert the signal from an analog signal to a digital signal and synchronizing said signal (See Column 10 Lines 29-67). Jeong teaches performing edge detection on a data

stream (See Page 9 Lines 5-13). When combined, the phase rotator of Shohara is used in conjunction with the edge detection of Jeong, as claimed in Claims 1 and 11. One of ordinary skill in the art at the time the invention was made would use the phase rotator of Shohara in conjunction with the device of Jeong to improve the frequency control resolution and thereby reduce the receiver frequency error (See Column 5 Lines 28-34 of Shohara).

3. Applicant has argued that there is "nothing in any of the references which allows the use of multiple samples to determine the approximate center of the resulting data bit" and that Jeong is "completely silent about data boundaries and the use of multiple samples to determine the same." As indicated in the rejections of Claim 9, from which Claim 10 depends, and Claim 19, from which Claim 20 depends, Jeong teaches using multiple samples to determine edges in a data stream (See Page 9 Lines 5-8). Specifically, Jeong teaches oversampling each bit of data three times. As indicated in the rejections of Claims 10 and 20, Jeong teaches using said multiple samples to determine the approximate center of said resulting data bit (See Page 10 Lines 23-27). Specifically, Jeong teaches passing only the bits which sample the centers of the incoming data from the oversampled three bits.

4. Applicant has argued that Gerowitz does not teach "three separate sets of latches as claimed in claims 3 and 13." The Examiner notes that Gerowitz teaches a first single bit data register (See Figure 2 Number L1'), a second single bit data register

(See Figure 2 Number L2'), and a third single bit data register (See Figure 2 Number L5) wherein data bits from the first and second single bit data registers are read out to a third single bit data register (See Column 4 Lines 38-41).

5. In response to Applicant's argument with regard to Claims 7 and 17 that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Hillis teaches that in using a shift register that takes two bits from an input signal and shifts them two bits at every clock pulse before shifting the accumulated bits out in parallel, the data transfer rate can be increased, since only half as many clock pulses are required because each transmission cycle accumulates two bits (See Column 4 Lines 8-10). As a result, power consumption is reduced since fewer clock transitions are required.

6. In response to Applicant's argument with regard to Claims 7, 8, 17, and 18 that the Examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the

obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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